IN THE TITLE

Please replace the title with the following:

A SCHEME FOR IMPROVING THE SIMULATION ACCURACY OF INTEGRATED CIRCUIT PATTERNS BY SIMULATION OF THE MASK

IN THE SPECIFICATION

Please amend the paragraph beginning on page 8, line 21 and ending on page 9, line 9 as follows:

(Presently Amended) In one embodiment, the present scheme involves simulating a photolithographic mask for fabrication of an integrated circuit, then simulating an image to be produced by that mask on a wafer. Afterwards, the mask may be corrected and/or optimized ~~and/or~~. Furthermore, the simulation or image ~~thereof~~ of the mask may be so corrected and/or optimized. Such correction/optimization may be accomplished by increasing or decreasing at least one magnitude or value of an optical proximity correction factor and/or a serif. The formats of the data input to or output from these simulation procedures are compatible with one another (e.g., bitmap format). Further, in other embodiments, corner rounding effects in an image produced by a mask may be corrected through simulation of optical proximity effects of the mask (e.g., effects of light having a wavelength approximately equal to four times a feature size-such as a line width or line spacing of the image). These corrections may be incorporated into the mask by adjusting an as-drawn layout of the mask as part of a CAD process.